

FIG. 2 PRIOR ART

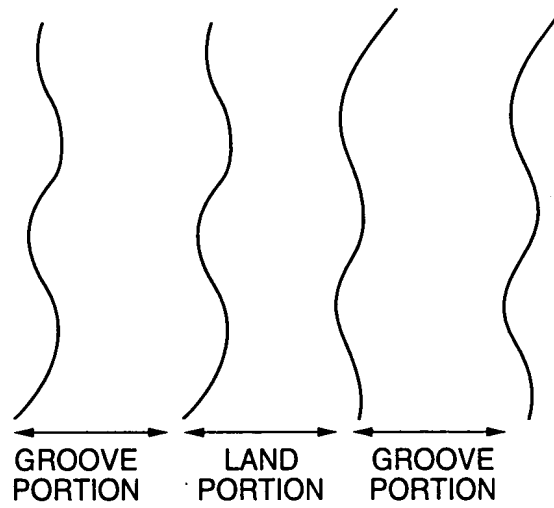


FIG. 3 PRIOR ART

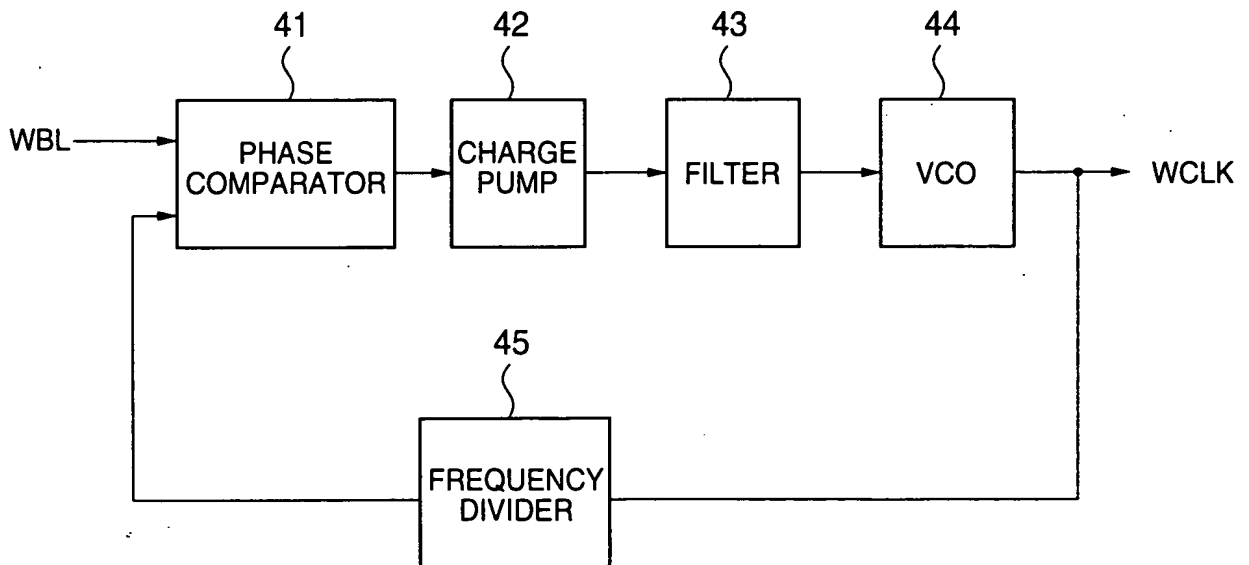


FIG. 4

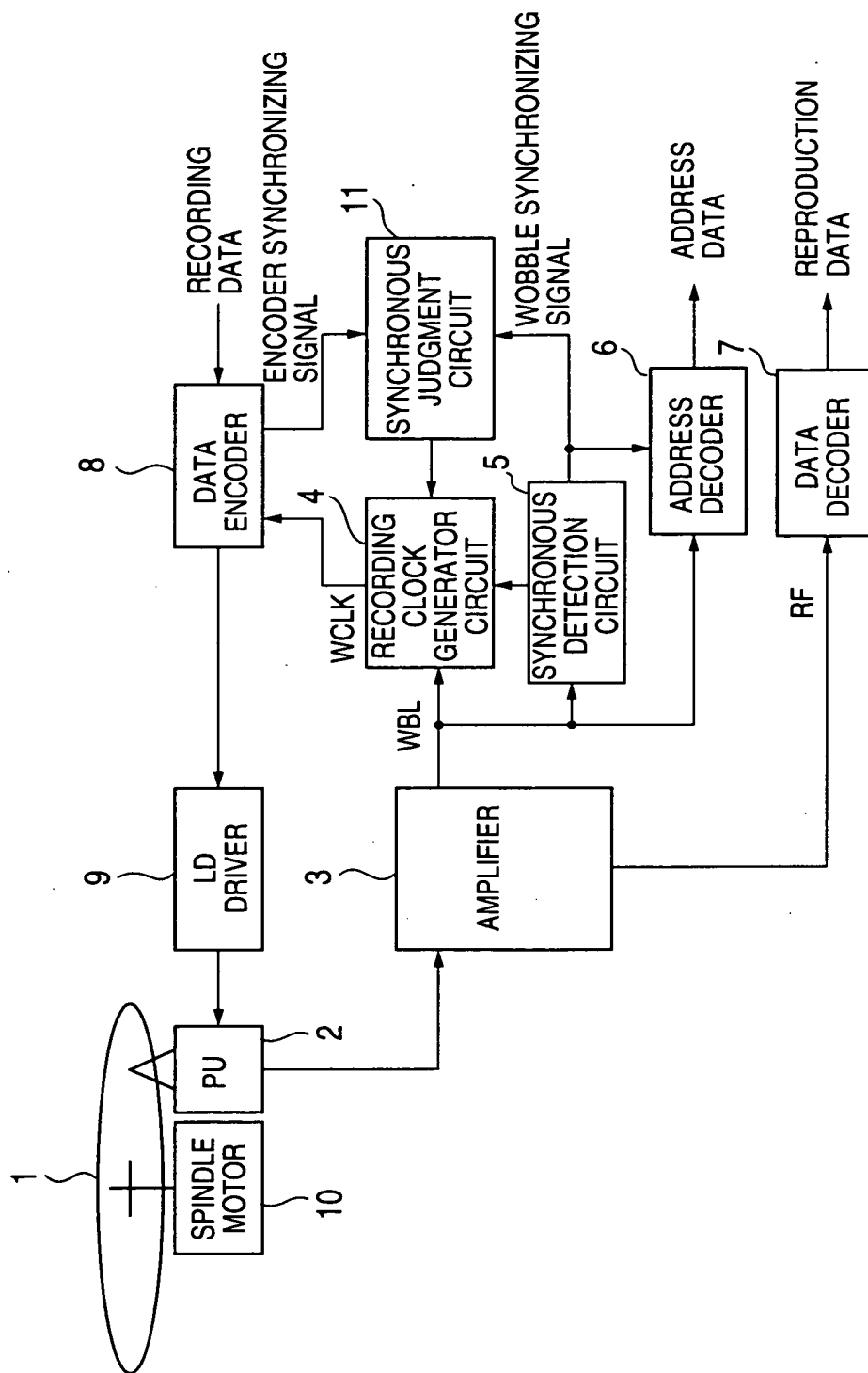


FIG. 5

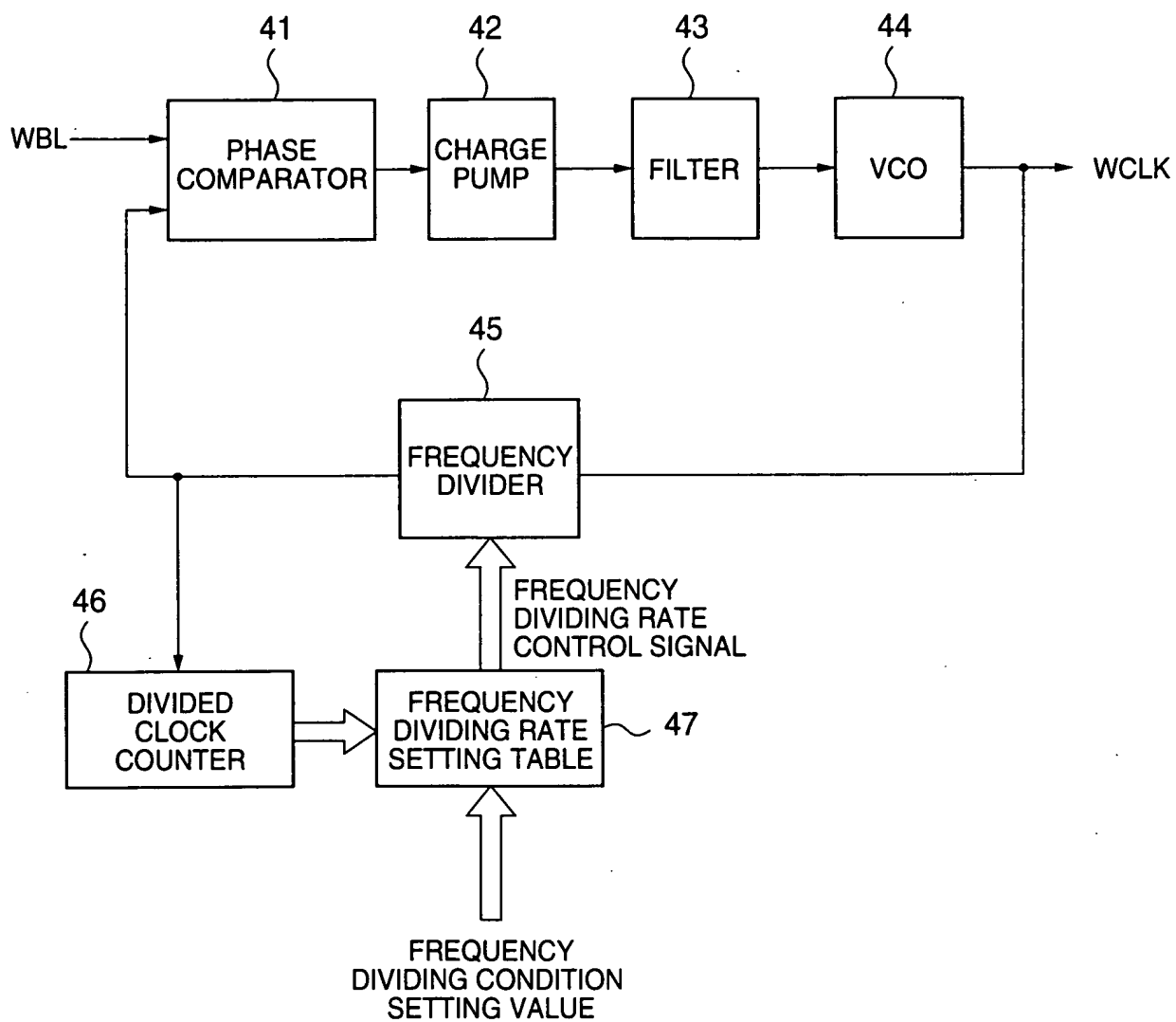


FIG. 6

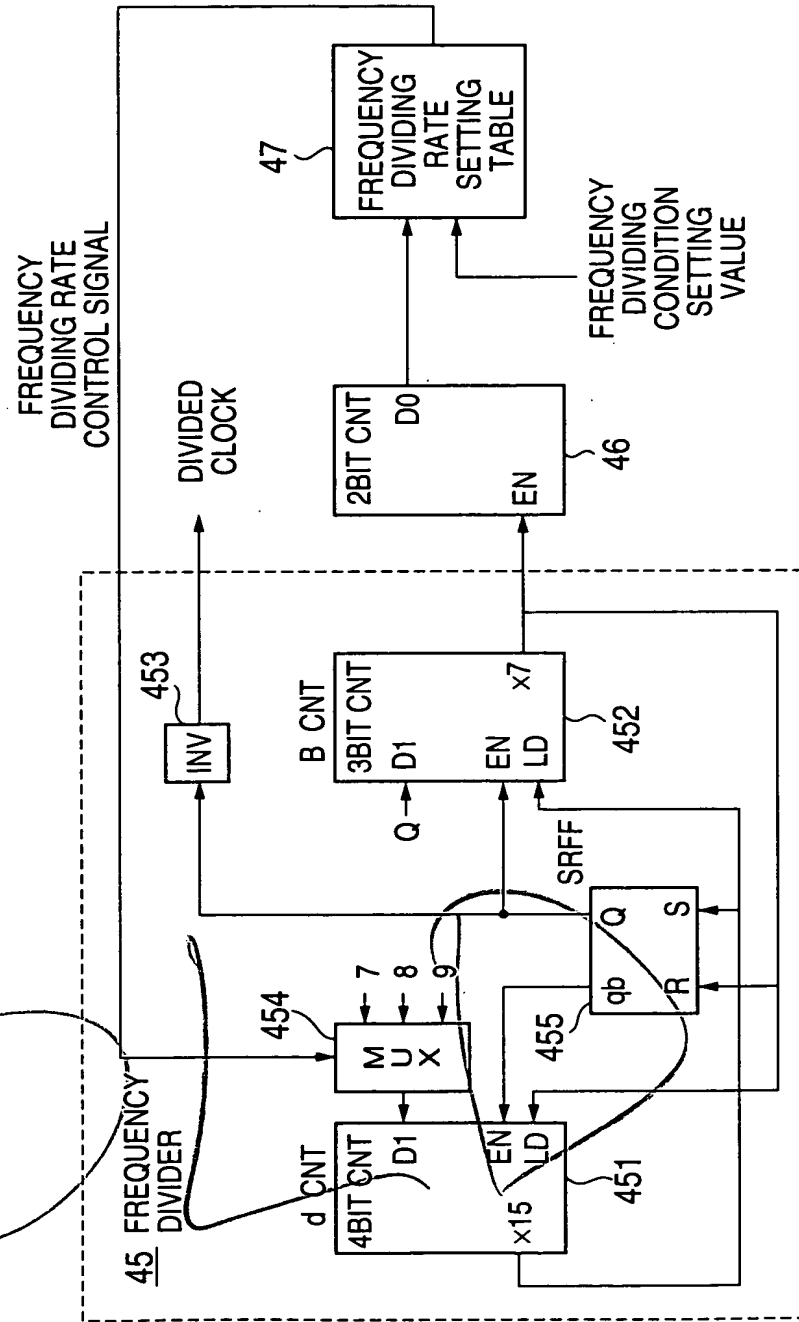


FIG. 7

FREQUENCY DIVIDING CONDITION SETTING VALUE	DIVIDED CLOCK COUNTER VALUE			
	0	1	2	3
0	ACNT	8 9 ... 15	8 9 10 ... 15	8 9 10 ... 15
	BCNT	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
	SRFF			
1	ACNT	7 8 9 ... 15	8 9 10 ... 15	8 9 10 ... 15
	BCNT	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
	SRFF			
2	ACNT	7 8 9 ... 15	7 16 17 ... 31	9 10 ... 15
	BCNT	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
	SRFF			
3	ACNT	7 8 9 ... 15	8 9 10 ... 15	9 10 ... 15
	BCNT	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
	SRFF			

DIVIDED  
CLOCK

DIVIDED	0	1	2	3	0	1	2	3
CLOCK								

WBL

DIVIDED CLOCK

FIG. 9

FREQUENCY DIVIDING CONDITION SETTING VALUE	DIVIDED CLOCK COUNTER VALUE				
	3	0	1	2	3
A CNT	9 10 ... 15	7 8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15
3→0 B CNT	7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
SRFF					
A CNT	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15
0→3 B CNT	7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
SRFF					



FIG. 10

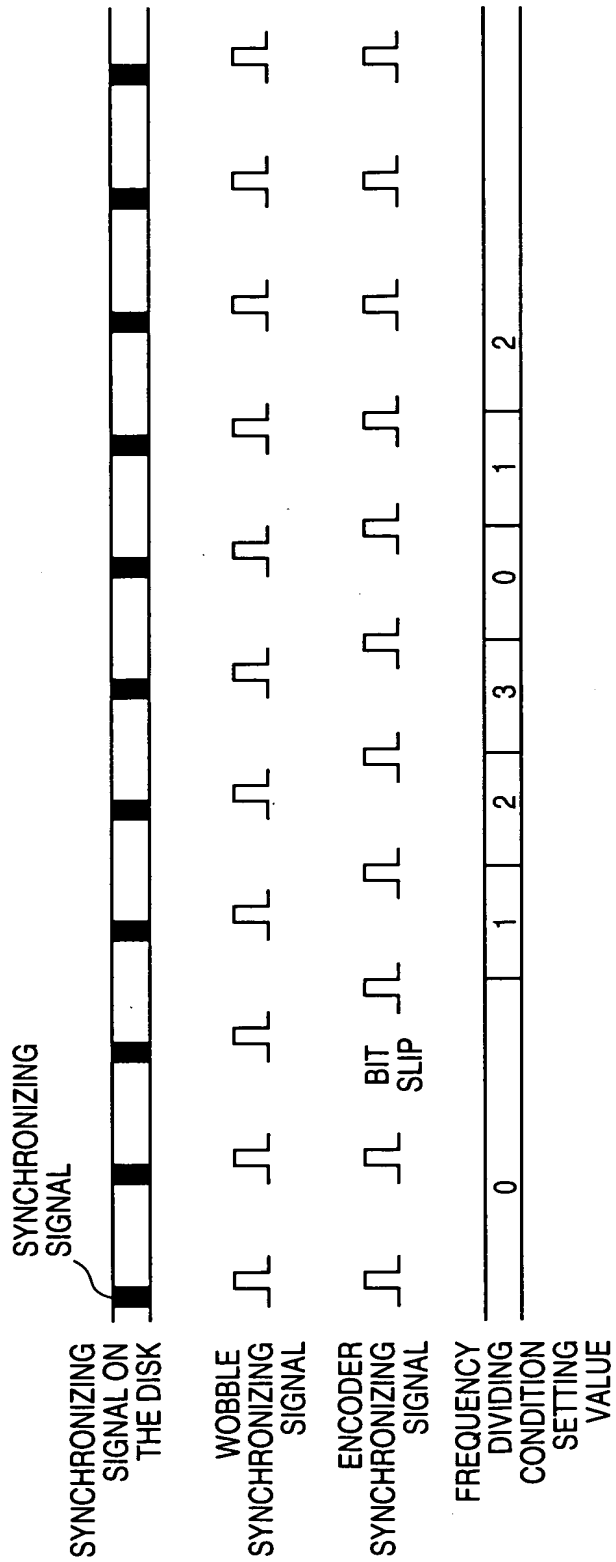




FIG. 12

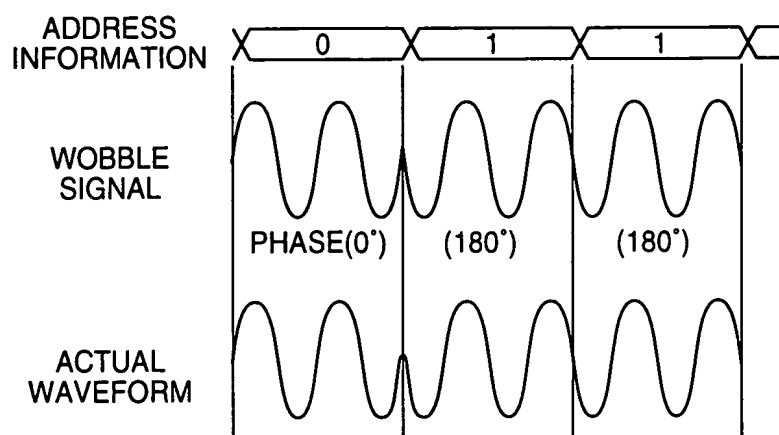


FIG. 13

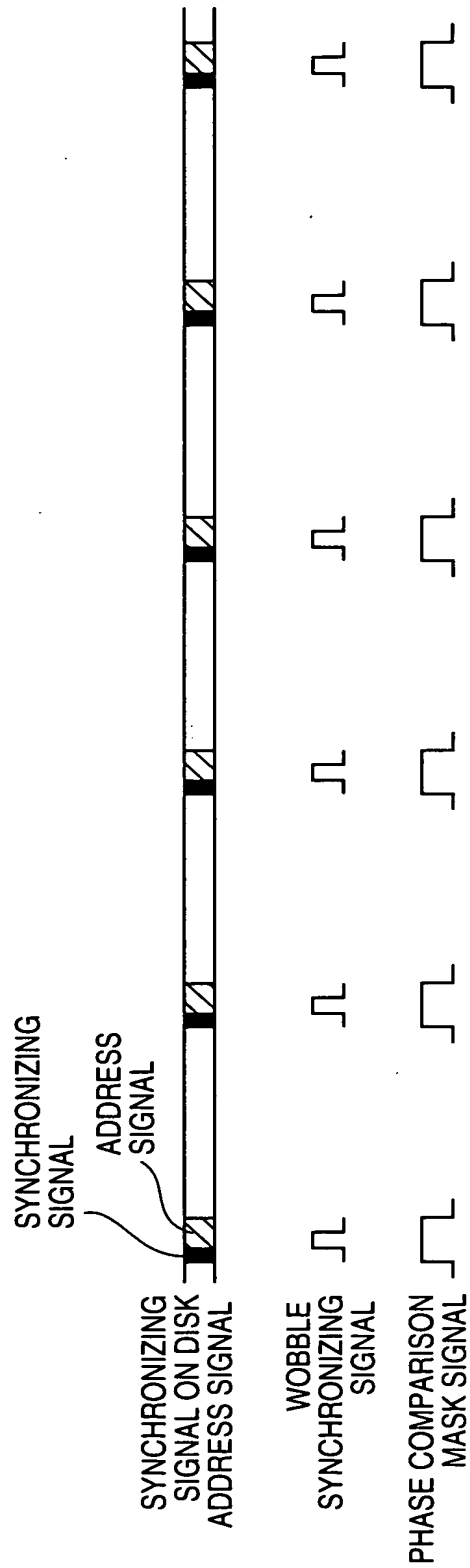


FIG. 14

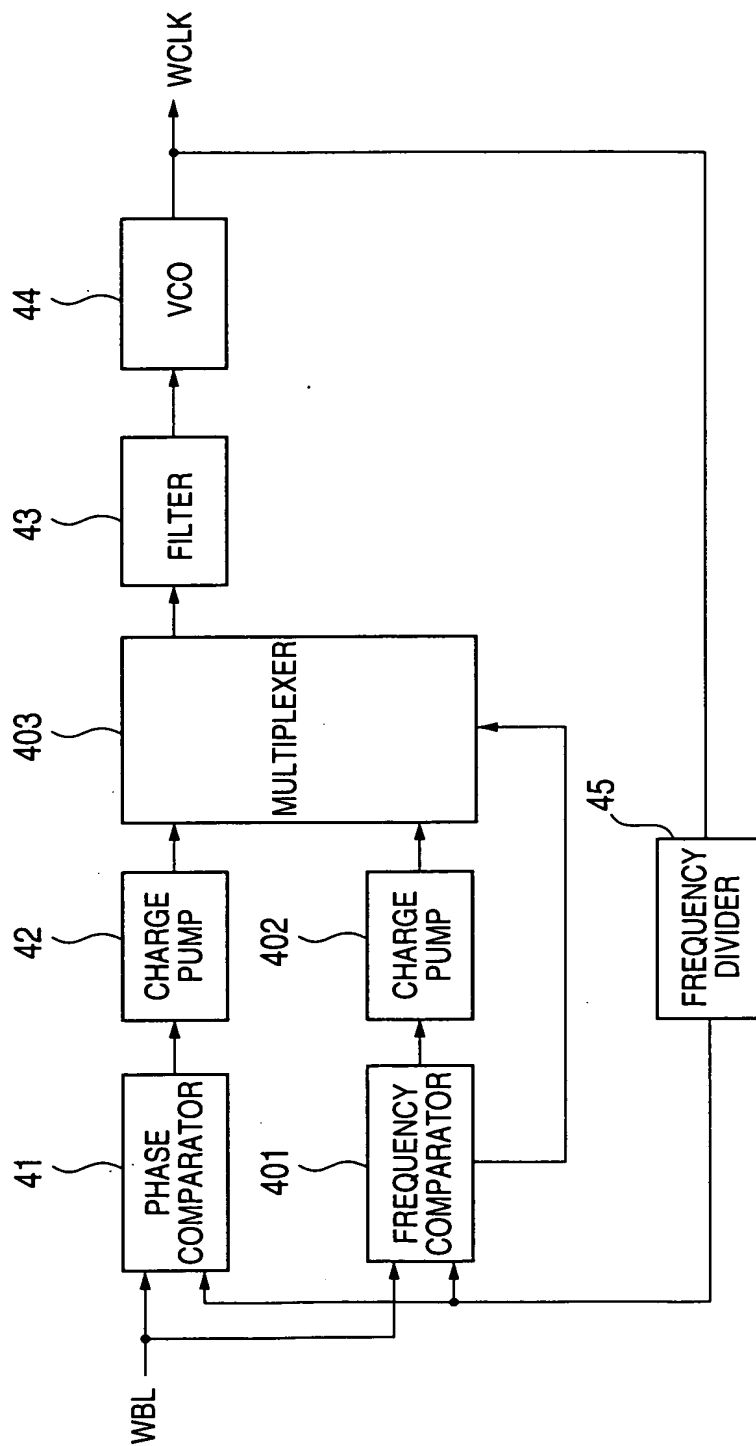


FIG. 15

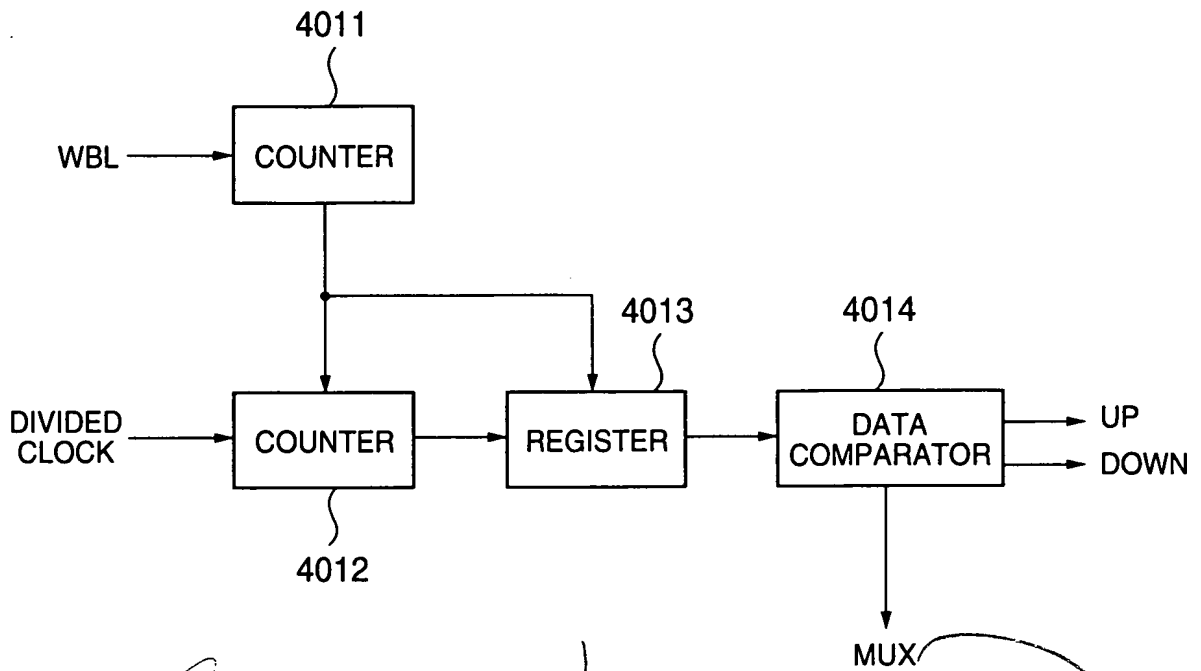


FIG. 16

